AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A dual chips stacked packaging structure, comprising:

a first chip, having an active surface and an opposing non-active surface, the active surface consisting of a central area and a peripheral area having a plurality of first bonding pads;

a lead frame, comprising a plurality of leads and a chip paddle having a first adhering surface and a second adhering surface, the first adhering surface adhered to the active surface of the first chip in such a way as to avoid contact with the first bonding pads;

a second chip, having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, the active surface consisting of a central area and a peripheral area having a plurality of second bonding pads, wherein the first and second chips adhere to either surface of the ~~same parts~~ center area of the chip paddle; and

a plurality of wires, wherein parts of the wires electrically connect with the first bonding pad and the leads, and parts of the wires electrically connect with the second bonding pad and the leads.

2. (Original) The structure as claimed in claim 1, wherein the first adhering surface of the chip paddle and the active surface of the first chip are adhered by a non-conductive solid or liquid adhesive.

3. (Original) The structure as claimed in claim 1, wherein the second adhering surface of the chip paddle and the non-active surface of the second chip are connected by a solid or liquid adhesive.

4. (Original) The structure as claimed in claim 1, wherein the wires are metal lines.

5. (Currently Amended) A dual chips stacked packaging structure, comprising:

a first chip, having an active surface and an opposing non-active surface, wherein the active surface consists of a central area and a peripheral area having a plurality of first bonding pads;

a lead frame comprising a plurality of leads and a chip paddle having a first adhering surface and a second adhering surface, the first adhering surface adhered to the active surface of the first chip in such a way as to avoid contact with the first bonding pads;

a second chip, having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, wherein the active surface consists of a central area and a peripheral area having a plurality of second bonding pads, wherein the first and second chips adhere to either surface of the ~~same parts~~ center area of the chip paddle;

a plurality of wires, parts of which electrically connect with the first bonding pad and the leads, and parts of which electrically connect with the second bonding pad and the leads; and

an encapsulation, covering the lead frame, the first chip, the second chip, and the wires.

6. (Original) The structure as claimed in claim 5, wherein each lead further comprises an inner lead covered by the encapsulation and outer lead extending beyond the encapsulation.

7. (Original) The structure as claimed in claim 5, wherein the first adhering surface of the chip paddle and the active surface of the first chip are adhered by a non-conductive solid or liquid adhesive.

8. (Original) The structure as claimed in claim 5, wherein the second adhering surface of the chip paddle and the non-active surface of the second chip are connected by a solid or liquid adhesive.

9. (Original) The structure as claimed in claim 5, wherein the wires are metal lines.

10. (Currently Amended) A dual chips stacked packaging structure, comprising:

a first chip, having an active surface and an opposing non-active surface, wherein the active surface consists of a central area and a peripheral area having a plurality of first bonding pads;

a lead frame, comprising a plurality of leads and a chip paddle having a first adhering surface and a second adhering surface, the first adhering surface adhered to the active surface of the first chip in such a way as to avoid contact with the first bonding pads, and each of the leads comprising a wire connecting surface and an opposing wire non-connecting surface;

a second chip, having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, wherein the active surface consists of a central area and a peripheral area having a plurality of second bonding pads, wherein the first and second chips adhere to either surface of the center area of the chip paddle;

a plurality of wires, parts of which electrically connect with the first bonding pad and the wire connecting surface of the leads, and parts of which electrically connect with the second bonding pad and the wire connecting surface of the leads; and

an encapsulation, covering the chip paddle, the second chip, the wire connecting surface of the leads, the active surface of the first chip, and the wires, with the non-active surface of the first chip and the total wire non-connecting surface of the leads exposed beyond the encapsulation.

11. (Original) The structure as claimed in claim 10, wherein each lead further comprises an inner lead covered by the encapsulation and outer lead extending beyond the encapsulation.

12. (Original) The structure as claimed in claim 10, wherein the first adhering surface of the chip paddle and the active surface of the first chip are adhered by a non-conductive solid or liquid adhesive.

13. (Original) The structure as claimed in claim 10, wherein the second adhering surface of the chip paddle and the non-active surface of the second chip are connected by a solid or liquid adhesive.

14. (Original) The structure as claimed in claim 10, wherein the wires are metal lines.

15. (Currently Amended) The structure as claimed in claim 11, wherein the non-active surface of the first chip exposed beyond the encapsulation remains exposed when the outer leads are attached to ~~an exterior device~~ second level package.

16. (Currently Amended) The structure as claimed in claim 11, wherein the wire non-connecting surface of the leads remains exposed when the outer leads are attached to ~~an exterior device~~ second level package.

17. (Original) The structure as claimed in claim 10, wherein the first and second chips adhere to either surface of the same parts of the chip paddle.

18. (Currently Amended) A dual chips stacked packaging structure, comprising:

a first chip, having an active surface and an opposing non-active surface, wherein the active surface consists of a central area and a peripheral area having a plurality of first bonding pads;

a lead frame, comprising a plurality of leads and a chip paddle having a first adhering surface and a second adhering surface, the first adhering surface adhered to the active surface of the first chip in such a way as to avoid contact with the first bonding pads, and each of the leads comprising a wire connecting surface and an opposing wire non-connecting surface;

a second chip, having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, wherein the active surface consists of a

central area and a peripheral area having a plurality of second bonding pads and the second adhering surface of the chip paddle contacts the central area of the second chip;

a plurality of wires, parts of which electrically connect with the first bonding pad and the wire connecting surface of the leads, and parts of which electrically connect with the second bonding pad and the wire connecting surface of the leads; and

an encapsulation, covering the chip paddle, the second chip, the wire connecting surface of the leads, the active surface of the first chip, and the wires, with the total wire non-connecting surface of the leads exposed beyond the encapsulation.

19. (Original) The structure as claimed in claim 18, wherein the first and second chips adhere to either surface of the same parts of the chip paddle.

20. (Original) The structure as claimed in claim 18, wherein each lead further comprises an inner lead covered by the encapsulation and outer lead extending beyond the encapsulation, and the wire non-connecting surface of the leads remains exposed when the outer leads are attached to an exterior device.

21. (New) A dual chips stacked packaging structure, comprising:

a first chip, having an active surface and an opposing non-active surface, wherein the non-active surface consists of a central area and a peripheral area having a plurality of first bonding pads;

a second chip, having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, wherein the non-active surface consists of a central area and a peripheral area having a plurality of second bonding pads and the second adhering surface of the chip paddle contacts the central area of the second chip;

a lead frame, comprising a plurality of leads and a chip paddle having a first adhering surface and a second adhering surface, the second adhering surface adhered to the non-active surface of the second chip in such a way as to avoid contact with the second bonding pads, and each of the leads comprising a wire connecting surface and an opposing wire non-connecting surface;

a plurality of wires, parts of which electrically connect with the first bonding pad and the wire connecting surface of the leads, and parts of which electrically connect with the second bonding pad and the wire connecting surface of the leads; and

an encapsulation, covering the chip paddle, the first chip, the wire connecting surface of the leads, the non-active surface of the second chip, and the wires, with the total wire non-connecting surface of the leads exposed beyond the encapsulation.

22. (New) The structure as claimed in claim 21, wherein the first and second chips adhere to either surface of the same parts of the chip paddle.

23. (New) The structure as claimed in claim 21, wherein each lead further comprises an inner lead covered by the encapsulation and outer lead extending beyond the encapsulation, and

the wire non-connecting surface of the leads remains exposed when the outer leads are attached to an exterior device.